**Logo

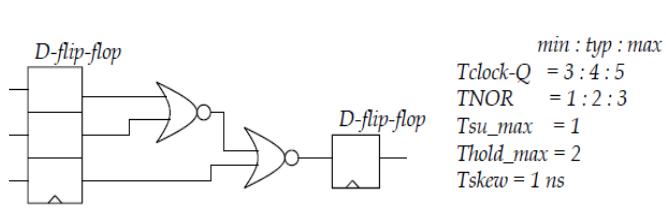
Description automatically generated San Francisco Bay University**

**EE461 Digital Design and HDL**

**Week#7 Timing Analysis in Verilog**

**IV. Exercises**

What is the fastest clock frequency given the following circuit and delay values? Is there potential for a hold violation?

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Assuming that the D flip-flops have a setup time (Tsu) of 0 and a hold time (Thold) of 2 (based on the Thold\_max given in the problem), the total delay through the circuit is:

Delay = Tsu\_max + TNOR + TNOR + Tclock-Q + Tskew

= 1 + 2 + 2 + 4 + 1

= 10 ns

To avoid hold violations, the output of the first D flip-flop needs to be stable for at least Thold\_max before the clock edge. Since the clock period (Tclk) is the inverse of the clock frequency (f), we can calculate the maximum clock frequency as:

f = 1 / Tclk <= (Tclk-Q - Tsu\_max - Thold\_max - TNOR - Tskew) / TNOR

= (5 - 1 - 2 - 2 - 1) / 2

= 0.5 GHz

Therefore, the maximum clock frequency for this circuit is 0.5 GHz.

Since the hold time requirement of the first flip flop is less than the hold time of 2, there is no potential for a hold violation.